nature photonics

Article

https://doi.org/10.1038/s41566-023-01309-7

On-chip optoelectronic logic gates operating in the telecom band

Received: 21 February 2023

Accepted: 12 September 2023

Published online: 30 October 2023

Check for updates

Ting He[1,2,6], Hui Ma[3,6], Zhen Wang[2,6], Qing Li[1,2] ✉, Shuning Liu[1], Shikun Duan[2], Tengfei Xu[2], Jiacheng Wang[1], Haitao Wu[1], Fang Zhong[1,2], Yuting Ye[4], Jianghong Wu[4], Shuo Lin[3], Kun Zhang[2], Piotr Martyniuk[2,5], Antoni Rogalski[5], Peng Wang[2], Lan Li[4], Hongtao Lin[3] ✉ & Weida Hu[1,2] ✉

Optoelectronic logic gates (OELGs) are promising building blocks for next-generation logic circuits and potential applications in light detection and ranging, machine vision and real-time video analysis. On-chip OELGs operating at telecom wavelengths are highly desirable for integration with the growing possibilities offered by silicon-based optoelectronics. However, at present operations are limited to linear logic functions in the ultraviolet or visible range and high-performance OELGs for multiple logic functions are lacking. Here we integrate up to three silicon waveguides with black phosphorus for optoelectronic logic operations at 1.55 μm. We demonstrate linear (AND, OR, NOT, NAND, NOR) and nonlinear (XOR and XNOR) OELGs by programming optical inputs into the waveguides and reading out electronic signals. The devices exhibit a responsivity as high as 0.35 A W^{-1} and a 3 dB bandwidth of 230 MHz. The combination of a photovoltaic OR gate and a voltage-switchable AND gate enables two-layer composite logic computing in the form (A + B)C. We also demonstrate symbol recognition, edge extraction, image fusion and encryption/decryption performed by these OELGs. This work paves the way for the development of new optoelectronic logic computing circuits.

Photons and electrons are fundamental transmission and computational carriers[1,2]. Traditionally, photodetectors convert optical data into electronic circuits for logic operations. With massive increases in data volumes, it is now necessary to improve the conversion efficiency of sensory nodes[3,4], especially for the telecom band. As a critical addition to all-electronic and all-optical logic devices, optoelectronic logic gates (OELGs) bring processing capability close to visual data sources[5,6]. Machine vision chips based on OELGs extract the features of imaging pictures through Boolean algorithms, which is expected to reduce redundant data substantially[7–10]. At this stage, the silicon-based optoelectronic platform offers the advantages of large-scale integration, high reliability and low cost[11]. Multifunctional OELGs integrated with silicon chips are highly desirable to promote miniaturization and integration[12]. Despite several reports on nanomaterial-based OELGs, almost all operated in ultraviolet and visible wavebands, which are not involved in the telecom bands[13–20]. In recent years, two-dimensional (2D) materials have shown excellent optical and electronic properties[21–23]. Benefiting from van der Waals interactions, synergistic combinations of 2D materials and silicon chips for photodetectors[24–30], modulators[31,32] and transistors[33] have achieved great success. The potential of this

[1]Hangzhou Institute for Advanced Study, University of Chinese Academy of Sciences, Hangzhou, China. [2]State Key Laboratory of Infrared Physics, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai, China. [3]State Key Laboratory of Modern Optical Instrumentation, College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China. [4]Key Laboratory of 3D Micro/Nano Fabrication and Characterization of Zhejiang Province, School of Engineering, Westlake University, Hangzhou, China. [5]Institute of Applied Physics, Military University of Technology, Warsaw, Poland. [6]These authors contributed equally: Ting He, Hui Ma, Zhen Wang. ✉e-mail: liqing@ucas.ac.cn; hometown@zju.edu.cn; wdhu@mail.sitp.ac.cn

https://doi.org/10.1038/s41566-023-01309-7

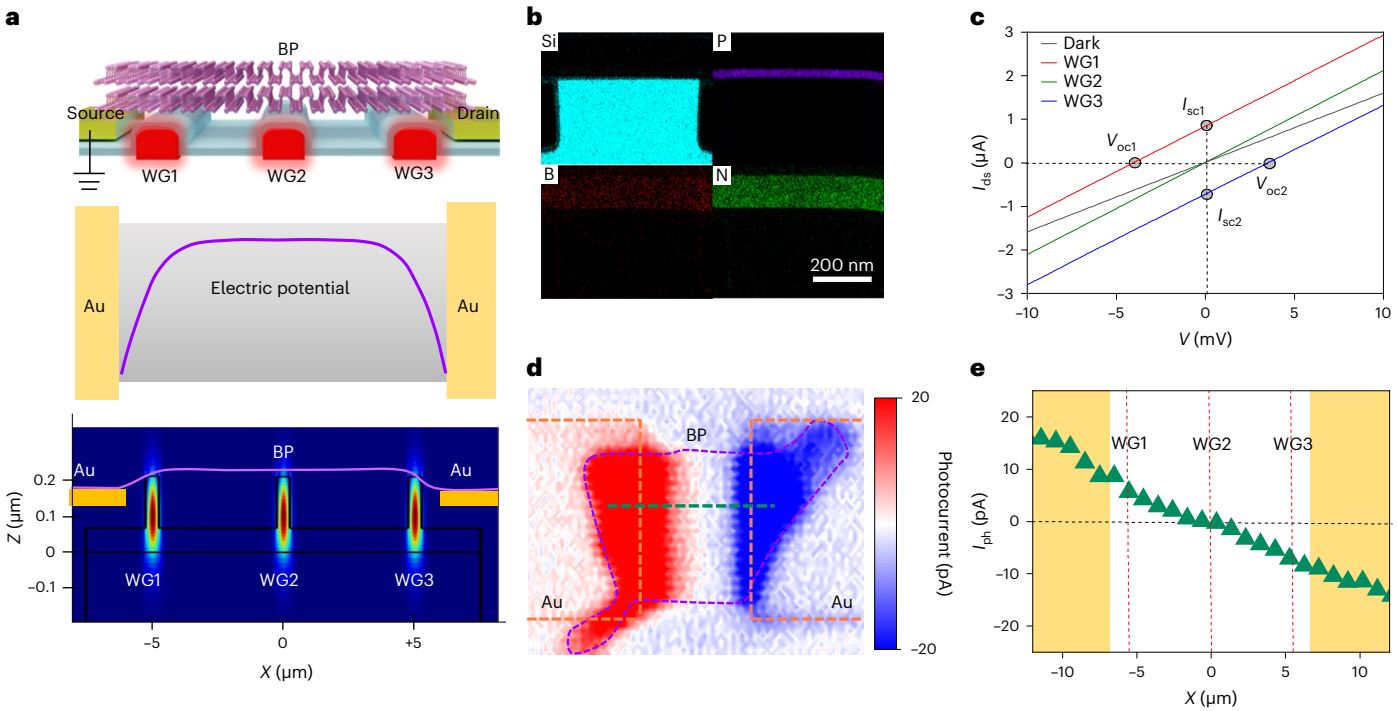


Fig. 1 | Au/BP/Au device integrated on a silicon photonic chip. a, Top: schematic of multifunctional OELGs integrated on a silicon chip. Middle: the spatial distribution of the electric potential at zero bias. Bottom: the light field distribution of the silicon photonic chip. **b**, EDS element mapping of the Au/BP/Au structure integrated on the waveguides. **c**, Output characteristics of the Au/BP/Au device in the dark and under 1.55 μm light illumination from the three waveguides. I_{ds}, drain–source current. I_{sc}, short-circuit current. V_{oc}, open-circuit voltage. **d**, Photocurrent mapping of the Au/BP/Au device. **e**, Photocurrent profile along the green dashed line in **d**. I_{ph}, photocurrent. Yellow shaded areas represent the Au electrodes.

combined platform remains unexplored in terms of enhancing the functional richness, integration efficiency and area utilization of OELGs.

In this work we developed a highly integrated optoelectronic logic architecture based on black phosphorus (BP) detection units integrated with a silicon-on-insulator photonic chip operating at 1.55 μm. Waveguides combined with localized electric potential regions form three detection units with different behaviours. Programming two detection units with opposite responses performs nonlinear XOR logic in a single device. The optimized responsivity and 3 dB bandwidth are 0.35 A W^{-1} and 230 MHz, respectively. Seven linear and nonlinear logic functions are realized with different input modes, including all-optical and mixed optical and electrical signal inputs. Combining devices with two input modes provides a two-layer composite logic computing solution. Edge extraction and image fusion are demonstrated based on XOR and OR OELGs. Real-time symbol recognition is realized by AND OELGs with mixed inputs.

Multi-waveguide integrated optoelectronic device

Figure 1a shows the design strategy of the multi-waveguide integrated optoelectronic device. The optical microscopy images and the fabrication method are shown in Extended Data Figs. 1 and 2. A two-terminal Au/BP/Au structure was placed on silicon ridge waveguides. We selected BP with a narrow bandgap of 0.3 eV due to the strong absorption of broad wavebands and high mobility. The thickness of the BP was approximately 11.7 nm. Taking full advantage of the vertical direction of the silicon platform[34], three ridge waveguides WG1, WG2 and WG3 were designed. The light field distribution of the silicon photonics chip is shown in the bottom panel of Fig. 1a. The distance between the Au electrode and WG1/WG3 was 1 μm, and the gap between the waveguides was 5 μm. The crosstalk and the loss of light absorbed by the metal electrode were negligible. More information on the chip layout can be found in Extended Data Fig. 3 and Supplementary Note 1. The relative electric potential in an Au/BP/Au device operating at zero bias was an inverted U-shape, obtained by technology computer-aided design simulations[35–37]. The positions of the waveguides were designed according to the localized potential distribution. The device was characterized by scanning transmission electron microscope (STEM) and energy dispersive X-ray spectroscopy (EDS) element mapping (Fig. 1b). The cross-section STEM images show that the BP was relatively flat, and a certain degree of bending was observed in the BP between the two waveguides, which occurred due to the 150 nm height difference from the substrate (Extended Data Fig. 4).

The output characteristics (I–V curves) of the Au/BP/Au device under photon triggering from three waveguides are shown in Fig. 1c. Illuminating WG1 or WG3 generated notable short-circuit currents and open-circuit voltages in the reverse direction. However, when WG2 was illuminated, the photocurrent was generated only when the bias voltage was applied. By introducing multiple waveguides, the integrated device formed three detection units with different behaviours. Two of them behaved with symmetrical positive and negative photoresponses. The central detection unit was only active under a bias voltage. The total output photocurrent of the device is the sum of the local directional current. Compared with discrete photodetectors used as switches, our OELGs improve area utilization and provide a minimum threefold increase in the integration efficiency.

Figure 1d shows the photocurrent mapping of the device at zero bias under 1.55 μm light illumination. Photocurrents with opposite direction were generated at the BP on the top of the two electrodes. Importantly, the photocurrent extended from the interface of the Au/BP to the channel. Figure 1e shows the photocurrent profile extracted along the green-dotted line in Fig. 1d. The photocurrent increased as the light spot moved away from the channel centre. When WG1 or WG3 were illuminated, photon-triggered electrons and holes

https://doi.org/10.1038/s41566-023-01309-7

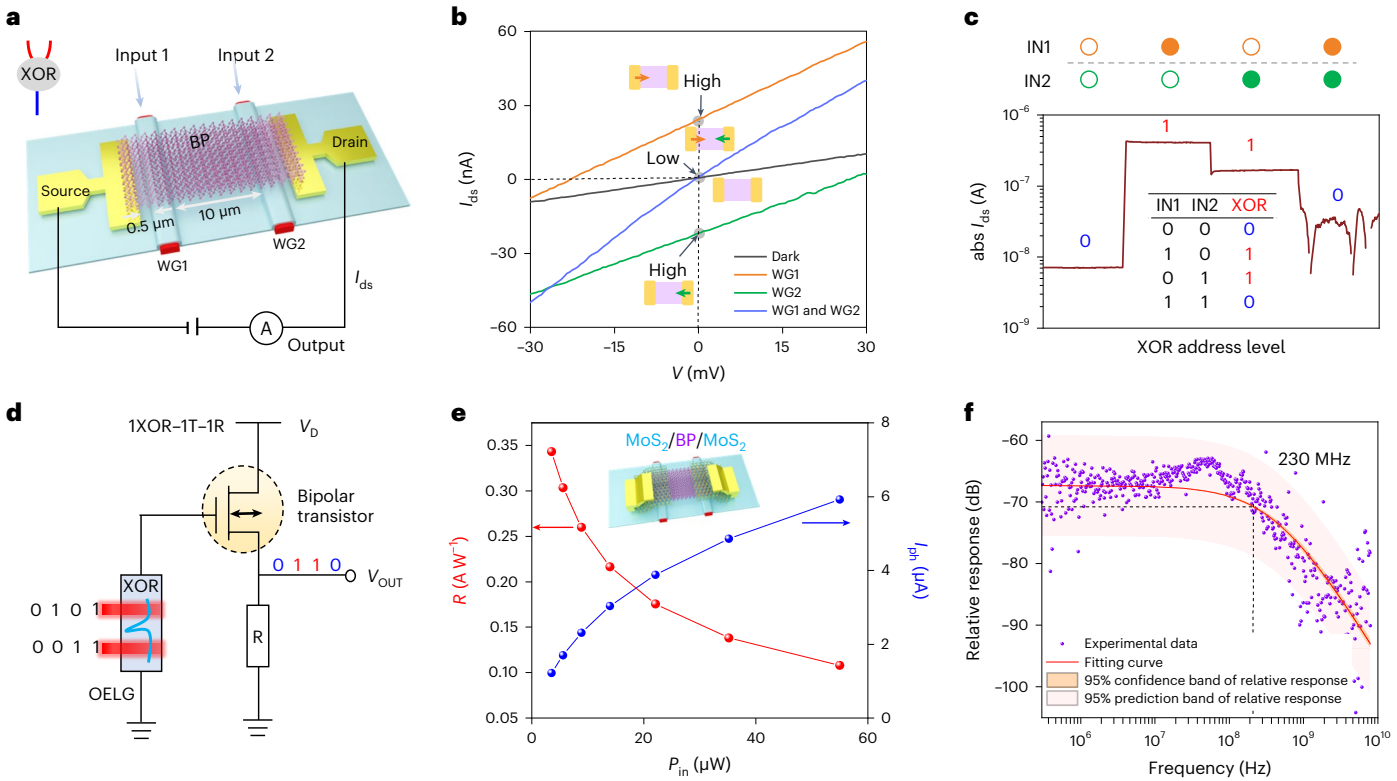


Fig. 2 | Design principles of OELGs with XOR operation in the telecom band. **a**, Schematic of the logic XOR gate structure with all-optical inputs. **b**, Output characteristics of the Au/BP/Au device in the dark and under 1.55 μm light illumination. Inset: schematic of photocurrent direction. **c**, Output current for four input states of the logic XOR gate. Inset: truth table for the XOR gate. abs, absolute. **d**, 1XOR–1transistor–1resistor circuit. V_D, drain voltage. V_{OUT}, output voltage. **e**, Photocurrent and responsivity of the MoS_2/BP/MoS_2 device as a function of incident power at zero bias. P_{in}, input power. Inset: diagram of the structure of the integrated MoS_2/BP/MoS_2 device. **f**, 3 dB bandwidth (230 MHz) of the MoS_2/BP/MoS_2 device at zero bias.

spread due to the carrier density gradient. The diffusion coefficient, mobility and density gradient led to diffusion differences between the photogenerated electrons and holes. After the carriers diffused to the depletion region, the built-in electric field of the Au/BP accelerated the drift of the photogenerated holes, whereas the photogenerated electrons were blocked (Extended Data Fig. 5). For WG2, the diffusion of carriers towards the source and drain regions was statistically equal. As a result, the net photocurrent was negligible.

OELG with XOR operation

The logic XOR function is one of the most complex 2 bit Boolean logic gates and requires 12 field-effect transistors in electronic circuits[7,8,38] and the nonlinear effects of semiconductor optical amplifiers in optical circuits[39]. We were able to achieve this function with the Au/BP/Au device integrated with two ridge waveguides. Figure 2a shows the operation conditions of optoelectronic logic XOR gates with all-optical inputs. The icon in the top left corner shows the input and output status: two red antennae on the head represent two optical signal inputs, and the blue tail represents electrical signal output. In the schematic structure of the device, WG1 and WG2 (with 10 μm spacing) served as inputs 1 and 2. Figure 2b shows output characteristics in the dark and under 1.55 μm light illumination. Four current states under zero bias are discussed in the inset of Fig. 2b: (1) when no photons are triggered, the current shows a relatively low level; (2) when WG1 or WG2 is photon triggered, the current shows a high level attributed to the photogenerated current; (3) when WG1 and WG2 are triggered together, the net photocurrent is cancelled, making the current level low. Thus, programming two detection units with positive and negative responses allows nonlinear OELG to be performed in a single device.

We experimentally measured the output current for the four input states of the logic XOR gate, as shown in Fig. 2c. The truth table is shown in the inset. Input signals of 0 or 1 indicate zero light power (unfilled circles) and high light power (filled circles), respectively. The first/second input signals (IN1/IN2) transmitted in WG1/WG2 are shown by orange and green circles, respectively. The absolute current was selected as the output signal (OUT). High and low absolute output currents represent OUT-1 and OUT-0. When a series of input signals with the sequential combination (IN-00, IN-01, IN-10, IN-11, bias of 0 V) is given, the device outputs XOR logic. Owing to the strong absorption of BP, the logic XOR gate has a high on-off ratio of nearly one order of magnitude. Compared with IN-00, the resistance value of IN-11 is small ($R_{IN\text{-}00} = 2.93 \times 10^6\ \Omega$, $R_{IN\text{-}11} = 7.47 \times 10^5\ \Omega$), and the corresponding thermal noise is larger ($i_{n\text{-}IN\text{-}00} = 7.5 \times 10^{-14}$ A Hz$^{-1/2}$, $i_{n\text{-}IN\text{-}11} = 1.5 \times 10^{-13}$ A Hz$^{-1/2}$). The stability of the IN-11 state also depends on the stability of the incident light. Consequently, the current fluctuation value of IN-11 is higher than that of IN-00. Despite these fluctuations, the logic functions remain unaffected. It is worth noting that our device has three output states: low, high positive and high negative. To make it work as a 2 bit XOR gate, we configured a 1XOR–1transistor–1resistor (1XOR–1T–1R) circuit (Fig. 2d). A bipolar transistor was needed to solve the problem of negative and positive states. The output current also transformed into voltage and entered the next stage.

The responsivity and processing speed are essential properties of OELGs. An MoS_2/BP/MoS_2 structure with a photodiode was fabricated to optimize the device performance (inset in Fig. 2e). The photocurrent of optoelectronic logic XOR gates reaches several microamperes. The responsivity was 0.35 A W^{-1} (Fig. 2e). The external quantum efficiency of MoS_2/BP/MoS_2 (28%) was 186 times larger than that of Au/BP/Au (0.15%).

https://doi.org/10.1038/s41566-023-01309-7

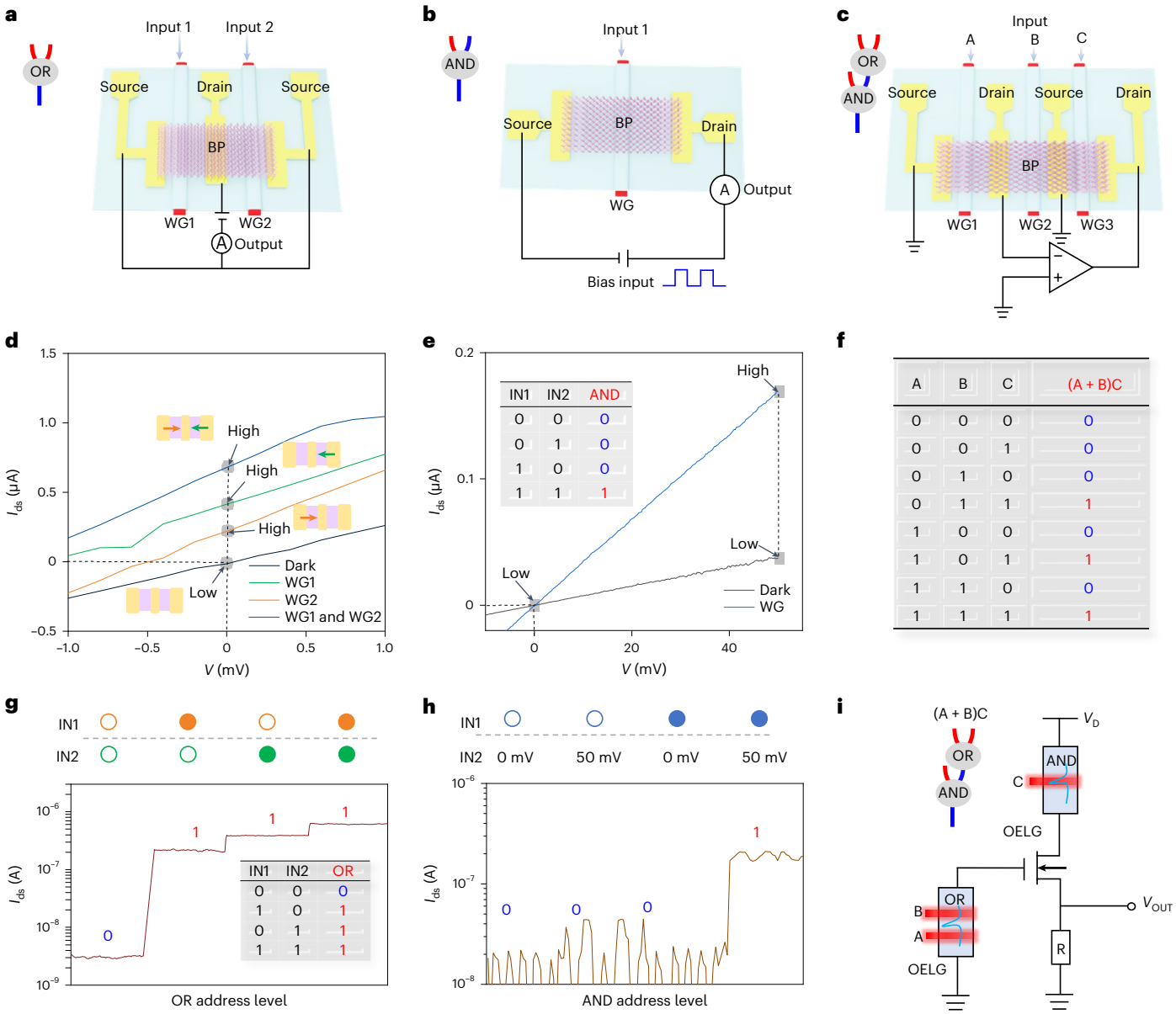


Fig. 3 | Design principle of OELGs with OR, AND and hybrid operation in the telecom band. a, Schematic of the logic OR gate with all-optical inputs. **b**, Schematic of the logic AND gate with mixed optical and electrical inputs. **c**, Schematic of the hybrid logic (A + B)C operation. **d**, Output characteristics of the OR device in the dark and under 1.55 μm light illumination. **e**, Output characteristics of the AND device in the dark and under 1.55 μm light illumination. Inset: truth table of the logic AND gate. **f**, Truth table of the (A + B)C function. **g**, Output current for four input states of the logic OR gate. Inset: truth table of the logic OR gate. **h**, Output current for four input states of the logic AND gate. **i**, Circuit of the hybrid (A + B)C logic operation.

Owing to the large built-in electric field from the PN junction, the 3 dB bandwidth reached 230 MHz (Fig. 2f). Extended Data Table 1 compares the performance of OELGs with other reported optoelectronic logic devices. Our device shows comparable responsivity and higher 3 dB bandwidth with low power consumption. Considering these two aspects, the MoS_2/BP/MoS_2 device offered the highest gain-bandwidth product. More information on the performance of the devices is shown in Extended Data Fig. 6.

OELGs with OR, AND and hybrid operation

Next we demonstrated OR logic function by changing the electric potential distribution. An M-shaped electric potential distribution was obtained by adding a drain electrode with 1 μm width in the middle of the Au/BP/Au structure to collect photocurrent, as shown in Fig. 3a. The optical microscopy image and layout of this device are shown in Extended Data Figs. 1 and 3. The equivalent circuit is two detection units with positive responses connected in parallel. Figure 3d shows the output characteristics, and four current states under zero bias were proposed to build a new logic function. As shown in Fig. 3g, when the sequence signal was IN-00, IN-01, IN-10, IN-11 (bias of 0 V), this device output OR logic. The truth table is shown in the inset. The ON/OFF ratio was more than one order of magnitude. The integrated platform offers high flexibility and competence for constructing OELGs with all-optical inputs by designing multi-electrodes and multi-waveguides.

In other cases, the optical signal needs to be logically processed with an electrical signal stored in the memorizer. OELGs with mixed inputs of optical and electrical signals are required. Fortunately, the photocurrent is influenced by the bias voltage. Figure 3b shows the

https://doi.org/10.1038/s41566-023-01309-7

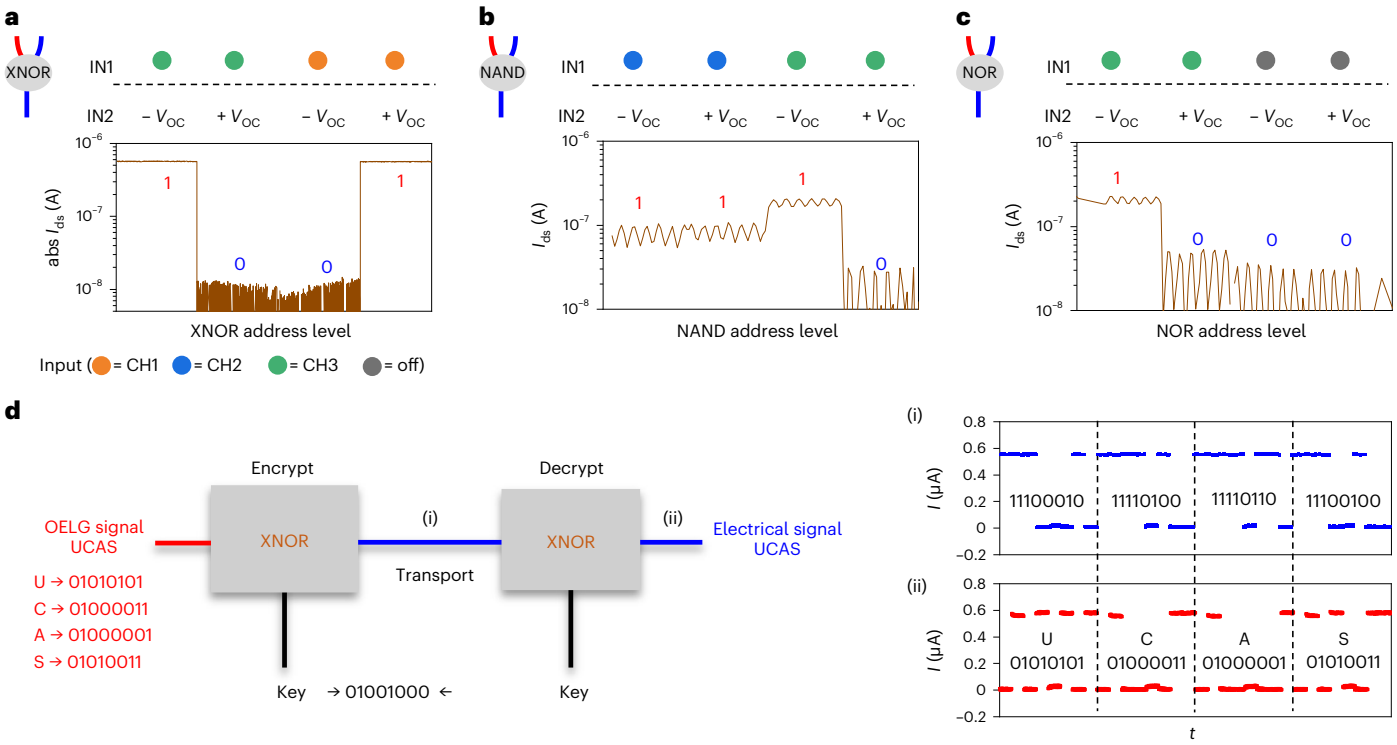


Fig. 4 | Experimental results for OELGs with XNOR, NAND and NOR operation in the telecom band. a–**c**, Output current for the four input states of XNOR (**a**), NAND (**b**) and NOR (**c**) gates. **d**, Left: schematic of XNOR gates used to encrypt/decrypt the signal. Right: experimental results for encrypted (i) and decrypted (ii) signals. *t*, time.

logic AND gate operation condition with mixed inputs of optical and electrical signals. The two head antennae of the icon are red and blue, representing the input signals in the optical and electrical domains, respectively; the blue tail represents the electrical signal output. The output curve of the device is shown in Fig. 3e. Under zero bias, currents both in the dark and under illumination are low. Under a bias voltage of 50 mV, the currents were 37 nA (dark, low state) and 0.16 μA (light illumination, high state), respectively. Experimentally, we measured the output current for the four input states. A first input signal (IN1) with a value of 0 or 1 indicated zero or high light power. A second input signal (IN2) indicated zero and positive bias voltage. The high and low output current represent OUT-1 and OUT-0, respectively. When sequence signals IN-00, IN-01, IN-10, IN-11 were sent, a logic AND gate could be constructed (Fig. 3h).

Owing to the input and output being located in different domains of the OELG, the traditional technique for creating multi-layer optoelectronic logic functions needs to send the electrical output signals to a modulator or a light source to transmit it onwards to the optical signal[40–43]. To build multi-layer logic functions, we combined an OR gate with all-optical inputs and an AND gate with mixed inputs (Fig. 3c). The higher open-circuit voltage originating from the output of the OR gate served as the electrical input to the AND gate. It provided a solution to perform (A + B)C. Figure 3f,i shows the truth table and configured circuit.

OELGs with XNOR, NAND and NOR operations

The electrical inputs could increase the modulation freedom of devices, enabling more complex logic functions. Three other OELGs with mixed inputs were demonstrated: XNOR, NAND and NOR. The device structures were consistent with that shown in Fig. 1a. A 1 × 2 fibre optical switch with one input and two output ports was used for photon switching between two waveguides (Extended Data Fig. 7a). The switching between the two waveguides defined the value of IN1 (0 and 1). Orange, blue and green circles represent the light conditions of WG1, WG2, and WG3, respectively. The grey circle represents no photons entering. Two symmetrical open-circuit voltages were chosen as the operating voltage points because the net photocurrent at V_{oc} cancels the dark current. The second input signal (IN2) with 0 or 1 indicated $-V_{oc}$ and $+V_{oc}$, respectively. As shown in Fig. 4a–c, logic XNOR, NAND and NOR gates were constructed after a series of input signals (IN-00, IN-01, IN-10, IN-11) was given. Extended Data Fig. 7 shows the detailed construction method.

Next we demonstrated the encryption/decryption scheme at the physical layer based on OELGs (Fig. 4d). A Boolean XNOR gate is the core device in the decision and comparison circuits, which can realize address recognition and data encryption/decryption. The signal 'UCAS' was compiled using American Standard Code for Information Interchange. Two signals (key as IN1, UCAS as IN2) were input to the XNOR gate, and an encrypted signal was output (Fig. 4d(i)). The encryption result was then returned to the XNOR gate for decryption (Fig. 4d(ii)). The bit error rate of our devices was on the order of 10^{-7}–10^{-8} (Supplementary Note 2). It is worth noting that the OELG also worked under free-space light illumination. The XNOR function was measured under spot illumination focused through an objective lens. The waveguide chip could also be integrated with other 2D semiconductors; for example, an Au/InSe/Au device was fabricated with the waveguides to demonstrate OR, AND and XNOR logic functions (Extended Data Fig. 8).

OELG-based imaging and image processing

Light detection and ranging (LIDAR) offers great advantages for intelligent transportation. Photodetectors and image processing units are important components of LIDAR, but these two components have so far only worked independently. To address this problem, we have

https://doi.org/10.1038/s41566-023-01309-7

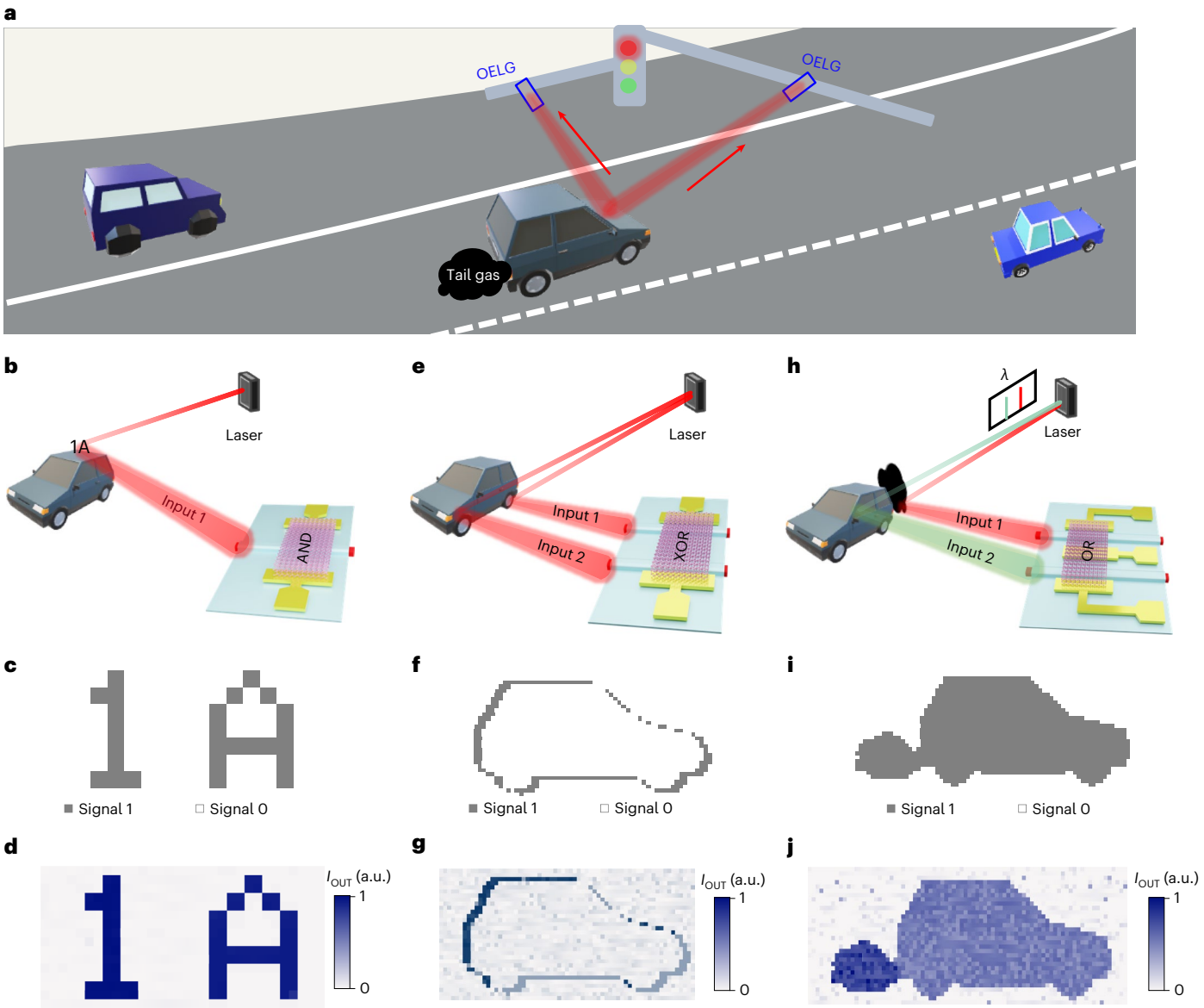


Fig. 5 | OELG-based imaging and image processing demonstrations. **a**, Potential application scenario of optoelectronic logic AND, XOR and OR gates. **b**, Schematic of an optoelectronic logic AND gate used for symbol recognition. **c**, 16 × 16 pixel simulation showing symbols 1A on the car. **d**, 16 × 16 pixel experimental result showing symbols 1A. **e**, Schematic of an optoelectronic logic XOR gate used for edge extraction. **f**, 64 × 32 pixel simulation showing the edge profile of the car. **g**, 64 × 32 pixel experimental result showing the edge profile of the car. **h**, Schematic of an optoelectronic logic OR gate used for image fusion. λ, wavelength. **i**, 64 × 32 pixel simulation showing image fusion of a car and exhaust fumes. **j**, 64 × 32 pixel experimental result showing image fusion of a car and exhaust fumes. Car models in **a**, **b**, **e**, **h** from TurboSquid.com.

developed OELGs for LIDAR demonstrations. OELGs are designed to achieve licence recognition, edge contour extraction and distinguish electric and gasoline vehicles, as shown in Fig. 5a. A beam of light scans the car's symbols (including letters and numbers). The reflected light in free space is collected by the coupler and temporally imported into the waveguide of the OELG. The BP detection unit converts the light signal into an electrical signal. At the same time, the target symbol '1A' is programmed pixel by pixel with the help of the bias voltage. Through the interaction between the light-stimulated and bias-triggered current signals, the optoelectronic AND logic gate achieves the desired 1A recognition (Fig. 5b). The symbol recognition process above was simulated by performing the AND logic operation between reference matrix α and target matrix β. A simulated output result for symbol 1A is shown in Fig. 5c. For the experiment, the signal generator loads the reference and target matrix signals on an OELG at the light and bias voltages, respectively. The output current by OELG is displayed on an oscilloscope after being pre-amplified (Fig. 5d). The experimental results demonstrate a close correlation between the recognition of the 1A symbol and the simulated outcome, which indicated that the device successfully performed AND logic operation and exhibited the ability to accurately recognize the symbol 1A.

To reduce the amount of data that needs to be stored, edge extraction of target objects is vital. Here, two beams of light were used to scan the car. The reflected signals from two adjacent positions were temporally introduced into two waveguides of the OELG (Fig. 5e). The OELG obtained the XOR logically processed results of the light-stimulated photocurrent from the two BP detection units, specifically capturing the edge profile of the car. The edge extraction of the car above was simulated as follows. First, we created a new car image (target matrices β) by shifting an existing car image (target matrices α) in a specific

direction by several pixels. Then, we conducted XOR logic operations on these two matrices, resulting in the generation of a simulation matrix as depicted in Fig. 5f. For the experiment, the signal generator loaded matrices α and β on two beams of light. The optoelectronic logic XOR gate obtained the superposition of the positive and negative response matrices. The output absolute current signal is shown in Fig. 5g, indicating that the device successfully executed XOR logic functions on two car images and could realize edge extraction of the target object.

Objects have distinctive fingerprint spectra. To detect the exhaust fume emissions from the car, the OELG utilized the infrared absorption properties of CO_2 and CH_4, as well as visible light reflection on the surface of the car. The different spectral characteristics of cars and exhaust fumes could be collected by the OELG (Fig. 5h). Two beams of light with different wavelengths scanned the car and its exhaust fumes, respectively. The reflected visible and infrared signals were temporally introduced into two waveguides. The OELG obtained logically processed results. The image fusion process above was simulated by performing OR logic operation of the car and exhaust fumes (Fig. 5i). In the experiment, the signal generator loaded the car matrix and exhaust fume matrix on two beams of light. The output current signal of the experimental result is shown in Fig. 5j. The above results indicate that an optoelectronic OR logic gate can realize image fusion of the target object successfully.

Discussion

In conclusion, we have demonstrated 2 bit Boolean OELGs based on BP integrated on silicon optoelectronic chips in the communication band. Extended Data Table 2 summarizes the function and degree of integration of our OELGs and other reported discrete devices. Compared with conventional discrete optoelectronic logic devices, our design exhibits distinct advantages in terms of function construction and the degree of integration. First, they are compatible with silicon optical links and capable of being integrated on the same chip as other optical components; second, chip-integrated light beams are smaller in scale, resulting in higher area utilization of the detection units; third, after integration with multi-waveguides, the rich local potential details of the BP device are available for programming, which improves the input efficiency of the OELGs. We have demonstrated symbol recognition, edge extraction, image fusion and encrypted communication with our OELGs. This strategy could be suitable for applications in artificial intelligence, optical computing and signal processing.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41566-023-01309-7.

References

1. Liu, C. et al. Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **15**, 545–557 (2020).
2. Caulfield, H. J. & Dolev, S. Why future supercomputing requires optics. *Nat. Photon.* **4**, 261–263 (2010).
3. Fu, Y. et al. All-optical logic gates based on nanoscale plasmonic slot waveguides. *Nano Lett.* **12**, 5784–5790 (2012).
4. Cheng, Z. et al. Device-level photonic memories and logic applications using phase-change materials. *Adv. Mater.* **30**, e1802435 (2018).
5. Zhang, K., Meng, D., Bai, F., Zhai, J. & Wang, Z. L. Photon-memristive system for logic calculation and nonvolatile photonic storage. *Adv. Funct. Mater.* **30**, 2002945 (2020).
6. Hao, Z., Yan, Y., Shi, Y. & Li, Y. Emerging logic devices beyond CMOS. *J. Phys. Chem. Lett.* **13**, 1914–1924 (2022).
7. Zeng, S. et al. An application-specific image processing array based on WSe_2 transistors with electrically switchable logic functions. *Nat. Commun.* **13**, 56 (2022).
8. Chen, H. et al. Logic gates based on neuristors made from two-dimensional materials. *Nat. Electron.* **4**, 399–404 (2021).
9. Zhou, F. et al. Optoelectronic resistive random access memory for neuromorphic vision sensors. *Nat. Nanotechnol.* **14**, 776–782 (2019).
10. Jang, H. et al. An atomically thin optoelectronic machine vision processor. *Adv. Mater.* **32**, e2002431 (2020).
11. Atabaki, A. H. et al. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature* **556**, 349–354 (2018).
12. Zhou, F., Chen, J., Tao, X., Wang, X. & Chai, Y. 2D materials based optoelectronic memory: convergence of electronic memory and optical sensor. *Research* **2019**, 9490413 (2019).
13. Wang, X. et al. Ultrafast, superhigh gain visible-blind UV detector and optical logic gates based on nonpolar a-axial GaN nanowire. *Nanoscale* **6**, 12009–12017 (2014).
14. Kim, J. et al. Photon-triggered nanowire transistors. *Nat. Nanotechnol.* **12**, 963–968 (2017).
15. Chen, J. et al. Work-function-tunable MXenes electrodes to optimize p-$CsCu_2I_3$/n-$Ca_2Nb_{3-x}Ta_xO_{10}$ junction photodetectors for image sensing and logic electronics. *Adv. Funct. Mater.* **32**, 2201066 (2022).
16. Pei, J., Wu, X., Liu, W. J., Zhang, D. W. & Ding, S. J. Photoelectric logic and in situ memory transistors with stepped floating gates of perovskite quantum dots. *ACS Nano* **16**, 2442–2451 (2022).
17. Kim, B. J. et al. Highly transparent phototransistor based on quantum-dots and ZnO bilayers for optical logic gate operation in visible-light. *RSC Adv.* **10**, 16404–16414 (2020).
18. Li, L. et al. Room-temperature valleytronic transistor. *Nat. Nanotechnol.* **15**, 743–749 (2020).
19. Boolakee, T. et al. Light-field control of real and virtual charge carriers. *Nature* **605**, 251–255 (2022).
20. Kim, Y. L. et al. Voltage-switchable photocurrents in single-walled carbon nanotube–silicon junctions for analog and digital optoelectronics. *Nat. Photon.* **8**, 239–243 (2014).
21. Youngblood, N., Chen, C., Koester, S. J. & Li, M. Waveguide-integrated black phosphorus photodetector with high responsivity and low dark current. *Nat. Photon.* **9**, 247–252 (2015).
22. Chen, Y. et al. Unipolar barrier photodetectors based on van der Waals heterostructures. *Nat. Electron.* **4**, 357–363 (2021).
23. Wu, P. et al. Van der Waals two-color infrared photodetector. *Light Sci. Appl.* **11**, 6 (2022).
24. Xia, F., Mueller, T., Lin, Y.-M., Valdes-Garcia, A. & Avouris, P. Ultrafast graphene photodetector. *Nat. Nanotechnol.* **4**, 839–843 (2009).
25. Mueller, T., Xia, F. & Avouris, P. Graphene photodetectors for high-speed optical communications. *Nat. Photon.* **4**, 297–301 (2010).
26. Gan, X. et al. Chip-integrated ultrafast graphene photodetector with high responsivity. *Nat. Photon.* **7**, 883–887 (2013).
27. Pospischil, A. et al. CMOS-compatible graphene photodetector covering all optical communication bands. *Nat. Photon.* **7**, 892–896 (2013).
28. Lin, H. et al. Chalcogenide glass-on-graphene photonics. *Nat. Photon.* **11**, 798–805 (2017).
29. Flöry, N. et al. Waveguide-integrated van der Waals heterostructure photodetector at telecom wavelengths with high speed and high responsivity. *Nat. Nanotechnol.* **15**, 118–124 (2020).
30. Wang, X., Cheng, Z., Xu, K., Tsang, H. K. & Xu, J.-B. High-responsivity graphene/silicon-heterostructure waveguide photodetectors. *Nat. Photon.* **7**, 888–891 (2013).

31. Shan, Z. et al. Phonon-assisted electro-optical switches and logic gates based on semiconductor nanostructures. *Adv. Mater.* **31**, e1901263 (2019).
32. Phare, C. T., Daniel Lee, Y.-H., Cardenas, J. & Lipson, M. Graphene electro-optic modulator with 30 GHz bandwidth. *Nat. Photon.* **9**, 511–514 (2015).
33. Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. *Nature* **573**, 507–518 (2019).
34. Behura, S. K., Wang, C., Wen, Y. & Berry, V. Graphene–semiconductor heterojunction sheds light on emerging photovoltaics. *Nat. Photon.* **13**, 312–318 (2019).
35. Ahmetoglu, M. & Akay, S. K. Determination of the parameters for the back-to-back switched Schottky barrier structures. *Curr. Appl. Phys.* **10**, 652–654 (2010).
36. Chiquito, A. J. et al. Back-to-back Schottky diodes: the generalization of the diode theory in analysis and extraction of electrical parameters of nanodevices. *J. Phys. Condens. Matter* **24**, 225303 (2012).
37. Osvald, J. Back-to-back connected asymmetric Schottky diodes with series resistance as a single diode. *Phys. Stat. Solidi A* **212**, 2754–2758 (2015).
38. Liu, C. et al. Small footprint transistor architecture for photoswitching logic and in situ memory. *Nat. Nanotechnol.* **14**, 662–667 (2019).
39. Zhihong, L. & Guifang, L. Ultrahigh-speed reconfigurable logic gates based on four-wave mixing in a semiconductor optical amplifier. *IEEE Photon. Technol. Lett.* **18**, 1341–1343 (2006).
40. Ashtiani, F., Geers, A. J. & Aflatouni, F. An on-chip photonic deep neural network for image classification. *Nature* **606**, 501–506 (2022).
41. Kim, W. et al. Perovskite multifunctional logic gates via bipolar photoresponse of single photodetector. *Nat. Commun.* **13**, 720 (2022).
42. Yang, C. M. et al. Bidirectional all-optical synapses based on a 2D Bi_2O_2Se/graphene hybrid structure for multifunctional optoelectronics. *Adv. Funct. Mater.* **30**, 2001598 (2020).
43. Li, M. et al. The fabrication of a self-powered $CuInS_2/TiO_2$ heterojunction photodetector and its application in visible light communication with ultraviolet light encryption. *J. Mater. Chem. C* **9**, 14613–14622 (2021).

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Springer Nature or its licensor (e.g. a society or other partner) holds exclusive rights to this article under a publishing agreement with the author(s) or other rightsholder(s); author self-archiving of the accepted manuscript version of this article is solely governed by the terms of such publishing agreement and applicable law.

© The Author(s), under exclusive licence to Springer Nature Limited 2023

Methods

Device fabrication

The device fabrication process is shown in Extended Data Fig. 2. A 220 nm silicon-on-insulator substrate was used to fabricate the photonics chips. First we patterned the photoresist (maN 2403) using electron beam lithography (Raith Voyager). Silicon was etched into three waveguides by inductively coupled plasma etching (OXFORD, Plasmapro100 Cobra 180). The Ti (5 nm)/Au (100 nm) electrode was then fabricated. Finally, 2D materials were transferred by the dry transfer method above three waveguides and two electrodes. Polypropylene propylene carbonate films were used as the adsorption layer, the viscosity of which changes with temperature (the films are less viscous at room temperature, increase in viscosity when heated to 40 °C and dissolve when heated to 120 °C). There are two effective ways to protect BP from oxygen and water. The first method uses a photoresist (PMMA) as the protection layer. The refractive index of PMMA (n = 1.4) is similar to that of silicon oxide. PMMA has little effect on the optoelectrical performance of passive silicon photonic devices. The second method is encapsulating BP with hexagonal boron nitride by dry transfer. The wide bandgap of boron nitride means that it will not absorb light in the communication band and at longer wavelengths.

Device performance measurement

A tunable C-band light (Santec TSL 550) was used as the source. An erbium-doped fibre application amplifier was used to boost the input power. The sourcemeter (Keithley 2450) supported the voltage and measured the current. The fibre measurement system is shown in Extended Data Fig. 7a.

Technology computer-aided design calculations

The photoelectric properties of the bilateral Schottky junction devices were numerically simulated with the Sentaurus technology computer-aided design. The structure consisted of two Schottky contacts and BP with the doping concentrations of 1×10^{17} cm^{-3}. The Schottky barrier was set as a variable to be more consistent with that of the experimental results.

Data availability

All of the data are presented in the main text and the Supplementary Information. The figures are also available via Figshare at https://doi.org/10.6084/m9.figshare.24056781. Data that support the findings of this study are available from the corresponding authors upon reasonable request. The 3D car models shown in Fig. 5 are available from TurboSquid at https://www.turbosquid.com/zh_cn/3d-model/free/cartoon-car?file_type=194%2C115. Source data are provided with this paper.

Acknowledgements

This work was financially supported by the Strategic Priority Research Program (B) of the Chinese Academy of Sciences (grant no. XDB0580000 to W.H.), the National Natural Science Foundation of China (grant nos. 62205082 to T.H., 62104053 to Q.L., 62105349 to Z.W., 62134009 to P.W. and 61975179 and 92150302 to H.L.), the Science and Technology Commission of Shanghai Municipality (grant nos. 23WZ2500400 and 21JC1406100 to W.H. and 22ZR1472300 to T.H.), the China Postdoctoral Science Foundation (grant no. 2021M700156 to T.H.), the Hangzhou Key Research and Development Program of China (grant no. 20212013B01 to W.H.) and the open fund of the State Key Laboratory of Infrared Physics (grant no. SITP-NLIST-ZD-2022-02 to H.L.). We thank ZJU Micro-Nano Fabrication Center at Zhejiang University.

Author contributions

W.H. and H.L. conceived and supervised the project. T.H., Z.W. and Q.L. designed the experiments. T.H. and H.M. fabricated the devices and performed the electrical and photoresponse characterizations. Q.L., P.M. and A.R. performed the technology computer-aided design calculations. S. Liu simulated the application demonstration. Z.W., S.D., S. Lin, F.Z., K.Z. and P.W. performed the experiments. J. Wang, Y.Y., J. Wu and L.L. assisted with the data analysis and interpretation. H.W. provided the circuit configuration. W.H., H.L., T.H., H.M. and T.X. wrote the manuscript. All authors discussed the results and revised the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Extended data is available for this paper at https://doi.org/10.1038/s41566-023-01309-7.

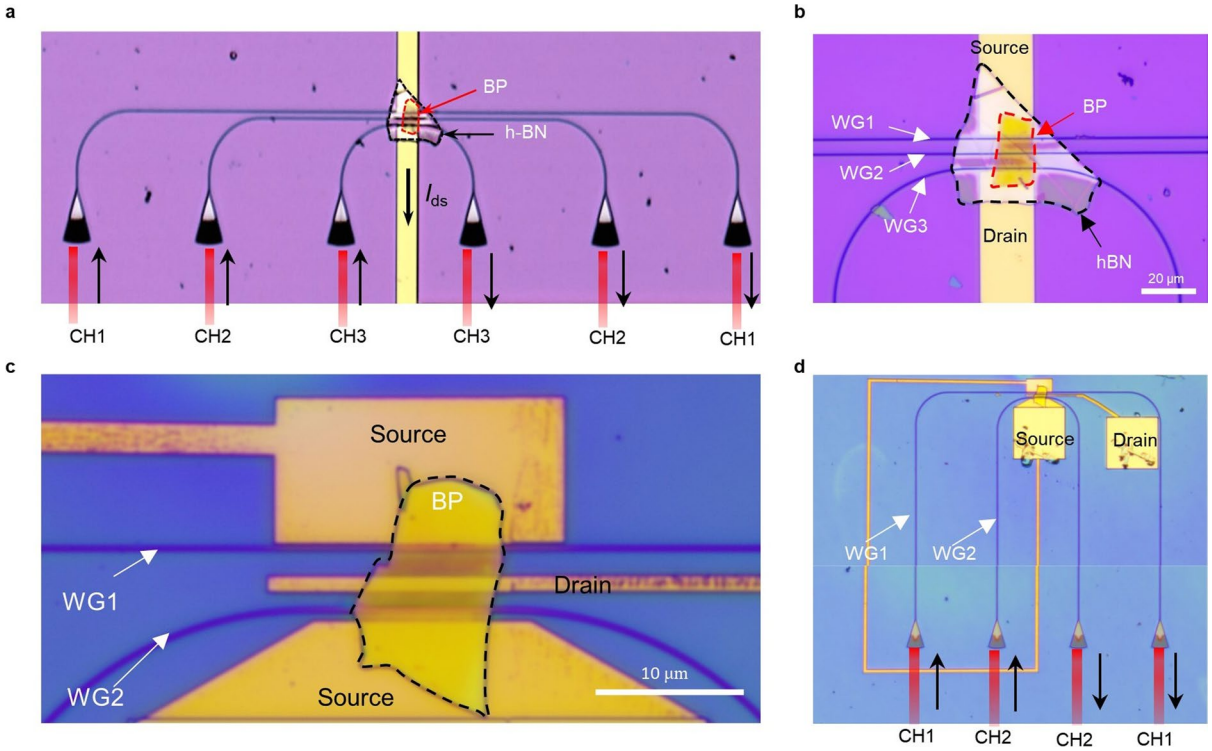
Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41566-023-01309-7.

Correspondence and requests for materials should be addressed to Qing Li, Hongtao Lin or Weida Hu.

Peer review information *Nature Photonics* thanks Ye Zhou and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

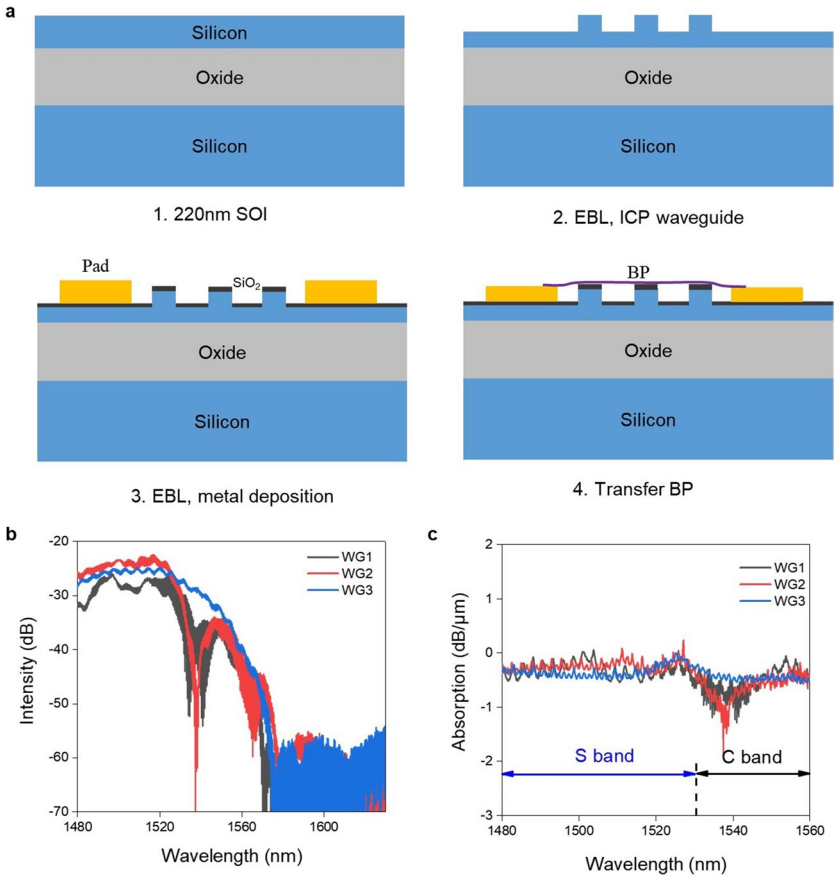
Reprints and permissions information is available at www.nature.com/reprints.

https://doi.org/10.1038/s41566-023-01309-7



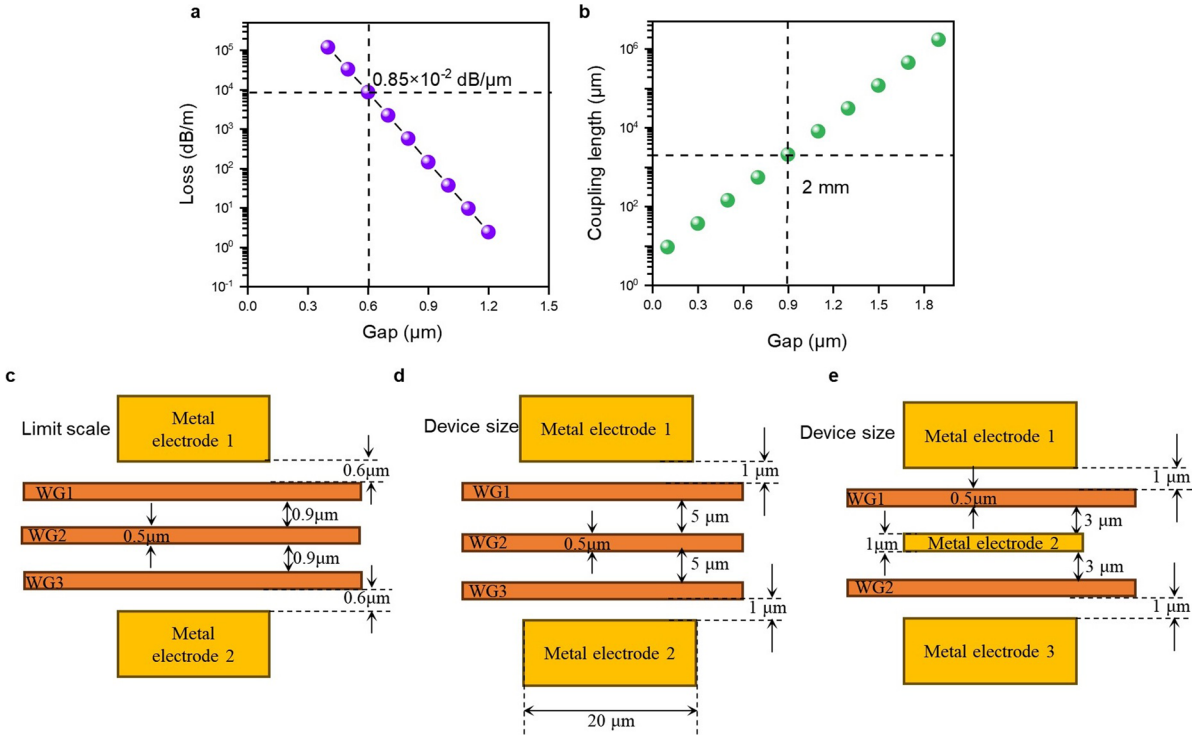
Extended Data Fig. 1 | Optical microscopy images of OELGs. (a) Optical microscopy image of integrated Au/BP/Au device with three waveguides. (b) Enlarged optical microscopy image of integrated Au/BP/Au device. (c) Enlarged optical microscopy image of optoelectronic logic AND gate. (d) Optical microscopy image of optoelectronic logic AND gate.

https://doi.org/10.1038/s41566-023-01309-7



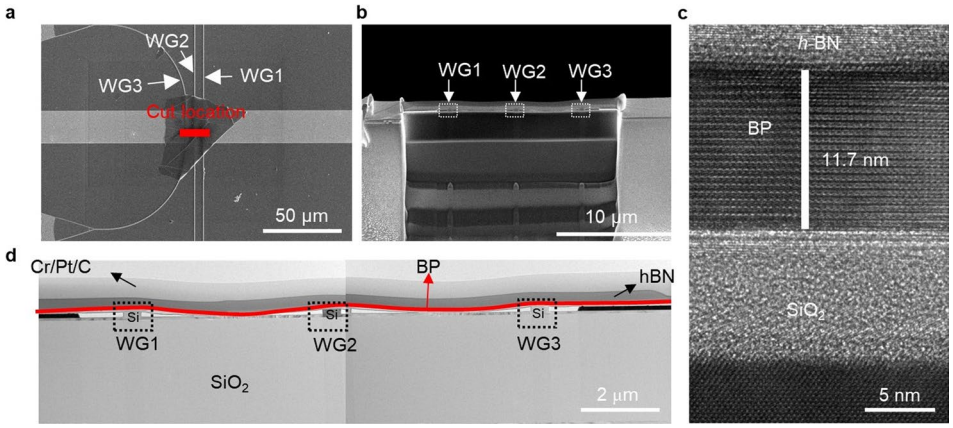
Extended Data Fig. 2 | Fabrication process of integrated device. (a) The devices were fabricated on the 220 nm SOI substrate. First, the photoresist (maN2403) was patterned through Electron Beam Lithography (EBL, Raith Voyager). And, the ridge waveguide (500 nm width) was etched by 150 nm through Inductively Coupled Plasma (OXFORD, Plasmapro100 Cobra 180). Then, the pad window (arp6200.13) was patterned, Ti (5 nm)/Au (100 nm) was deposited. Finally, BP was transferred by the dry method above three waveguides and two electrodes. The h-BN or PMMA was used as the passivation layer to protect BP. Grating couplers were used as fiber-to-waveguide couplings with a period of 0.67 μm, and a duty cycle of 0.5. (b) Transmission spectrum of WG1, WG2, and WG3. (c) Absorption of BP as a function of the wavelength. Due to the narrow bandgap, BP has a stable absorption at the S and C bands.

https://doi.org/10.1038/s41566-023-01309-7



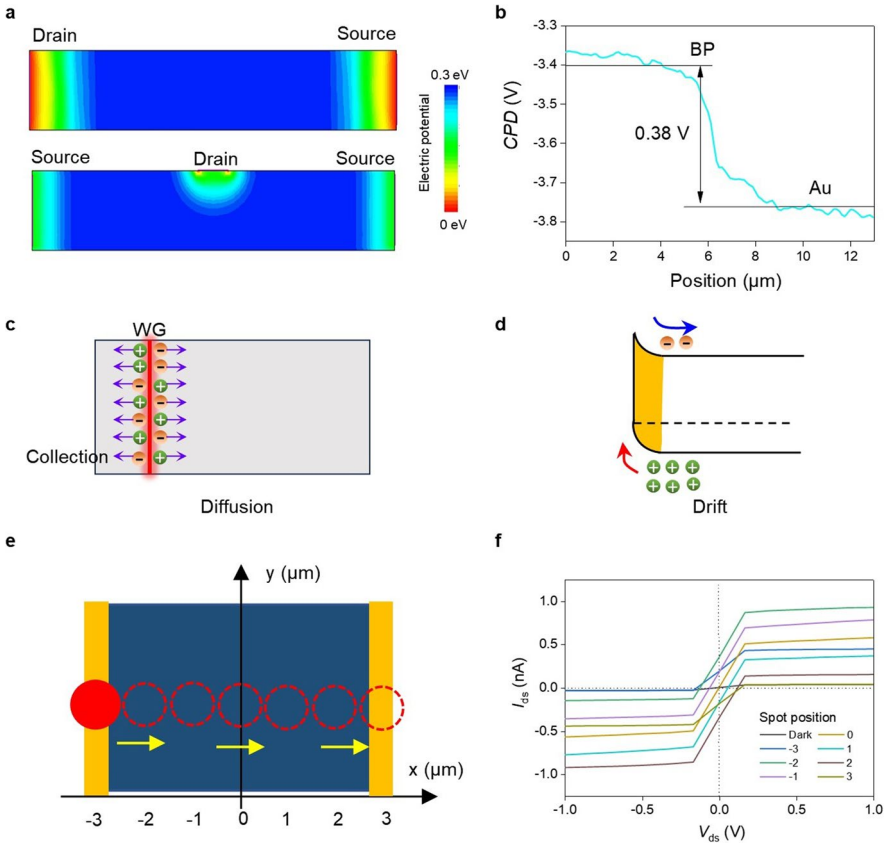
Extended Data Fig. 3 | Layout of waveguide chip. (a) Optical loss as a function of the gap between waveguide and metal electrode. (b) Relationship of coupling length and gap between two waveguides. (c) Limit scale of three waveguide device with three waveguides. (d) The size of fabricated Au/BP/Au device with three waveguides. (e) The size of fabricated optoelectronic logic AND device.

https://doi.org/10.1038/s41566-023-01309-7



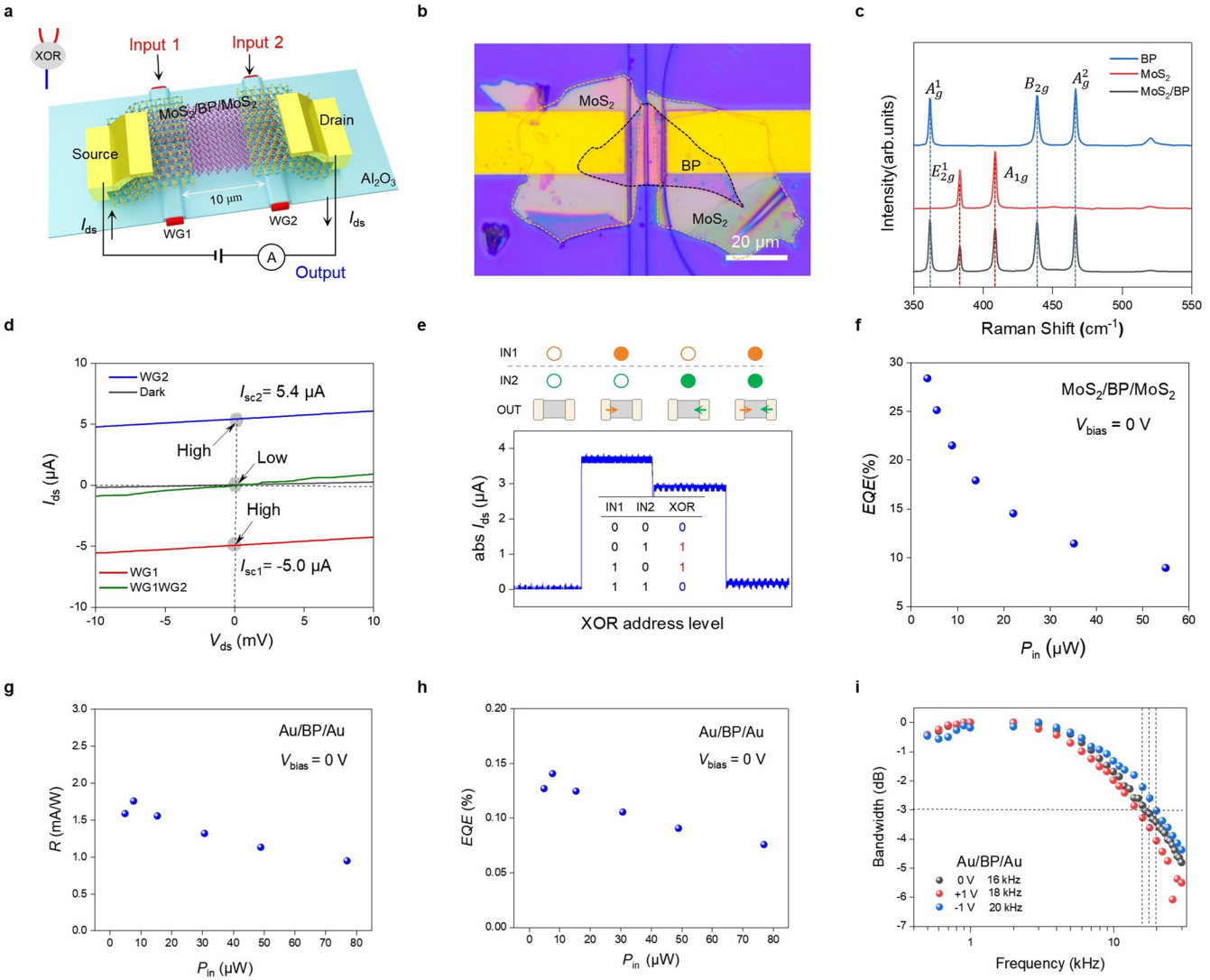
Extended Data Fig. 4 | STEM results of integrated Au/BP/Au device. (a) SEM picture of Au/BP/Au device from the top view. (b) Cross-section scanning transmission electron microscope (STEM) image of Au/BP/Au device. (c) The thickness of BP is approximately 11.7 nm. (d) Enlarged STEM image of Au/BP/Au device.

https://doi.org/10.1038/s41566-023-01309-7



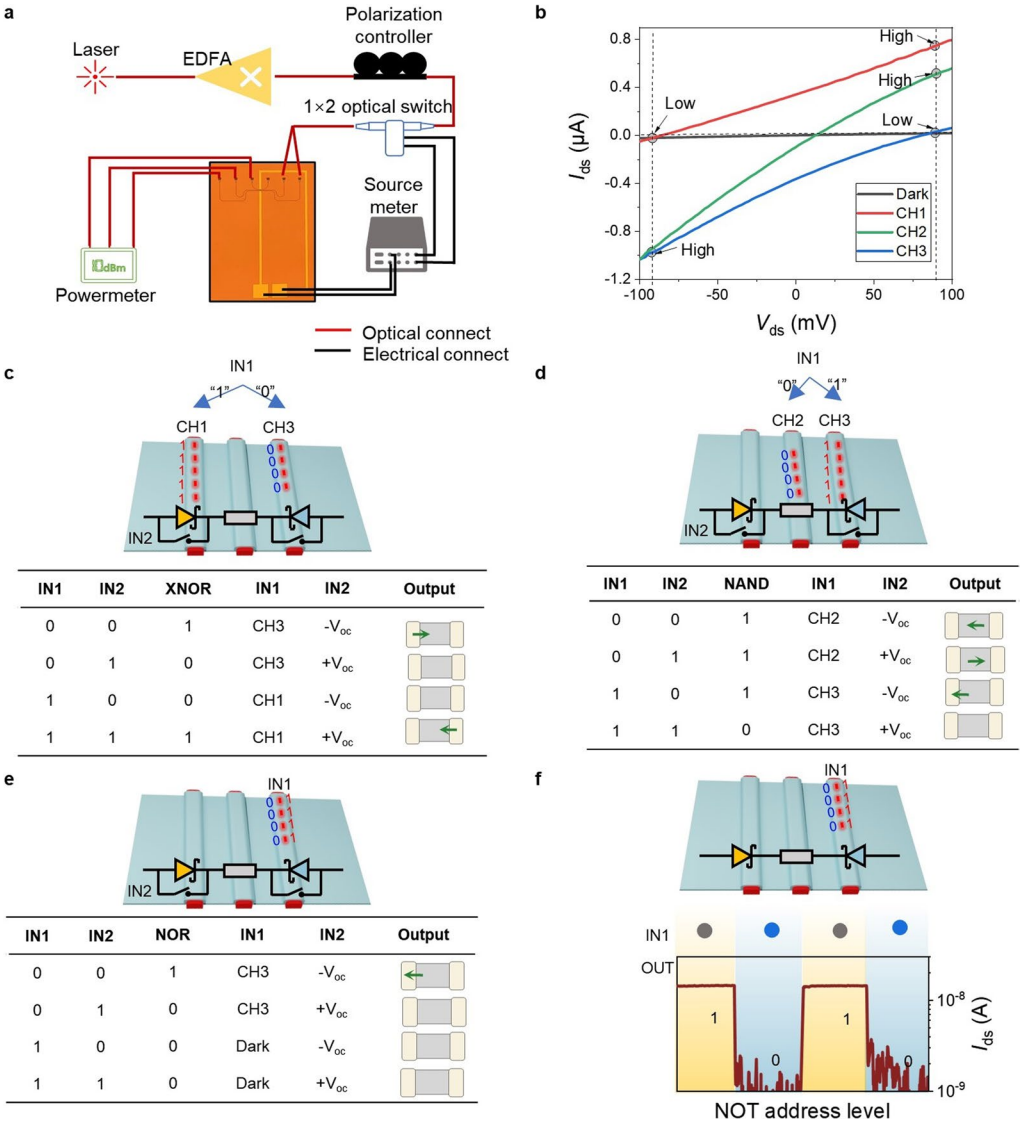
Extended Data Fig. 5 | Simulated optoelectronic characteristics of OELGs. (a) Electric potential distribution of Au/BP/Au device and an "M" shape potential distribution of optoelectronic logic AND device simulated by Sentaurus TCAD. (b) Surface potential difference between BP and Au by Kelvin probe force microscopy. The results show that the work function of BP is around 0.38 eV higher than that of Au. The work function difference between BP and Au is smaller than that of the theoretical value, which may be attributed to the surface oxidation of BP. (c) Diffusion process of photogenerated electrons and holes in Au/BP/Au device under WG1 triggering. (d) Energy band diagram for drift process of photogenerated electrons and holes in Au/BP/Au device under WG1 triggering. (e) Simulated structure of Au/BP/Au device and illumination mode. The light spot diameter is approximately 1 μm. (f) Simulated I-V curves of Au/BP/Au device under light illumination of different spot positions.

https://doi.org/10.1038/s41566-023-01309-7



Extended Data Fig. 6 | Performance of MoS2/BP/MoS2 and Au/BP/Au for XOR gate. (a) Schematic of MoS_2/BP/MoS_2 device with logic XOR function. (b) Optical microscope image of MoS_2/BP/MoS_2 device. (c) Raman spectra of BP, MoS_2, and overlapped region. (d) Output characteristics of device in dark and under 1.55 μm light illumination. (e) Output current of logic XOR gate with four input states. Inset is truth table of logic XOR. (f) External quantum efficiency (EQE) as a function of incident light power for MoS_2/BP/MoS_2 device at zero bias voltage. (g) Responsivity of Au/BP/Au device as a function of the incident light power at zero bias voltage. (h) EQE of Au/BP/Au device as a function of the incident light power at zero bias. (i) 3 dB bandwidth of Au/BP/Au device under 1.55 μm light illumination from WG1.

https://doi.org/10.1038/s41566-023-01309-7



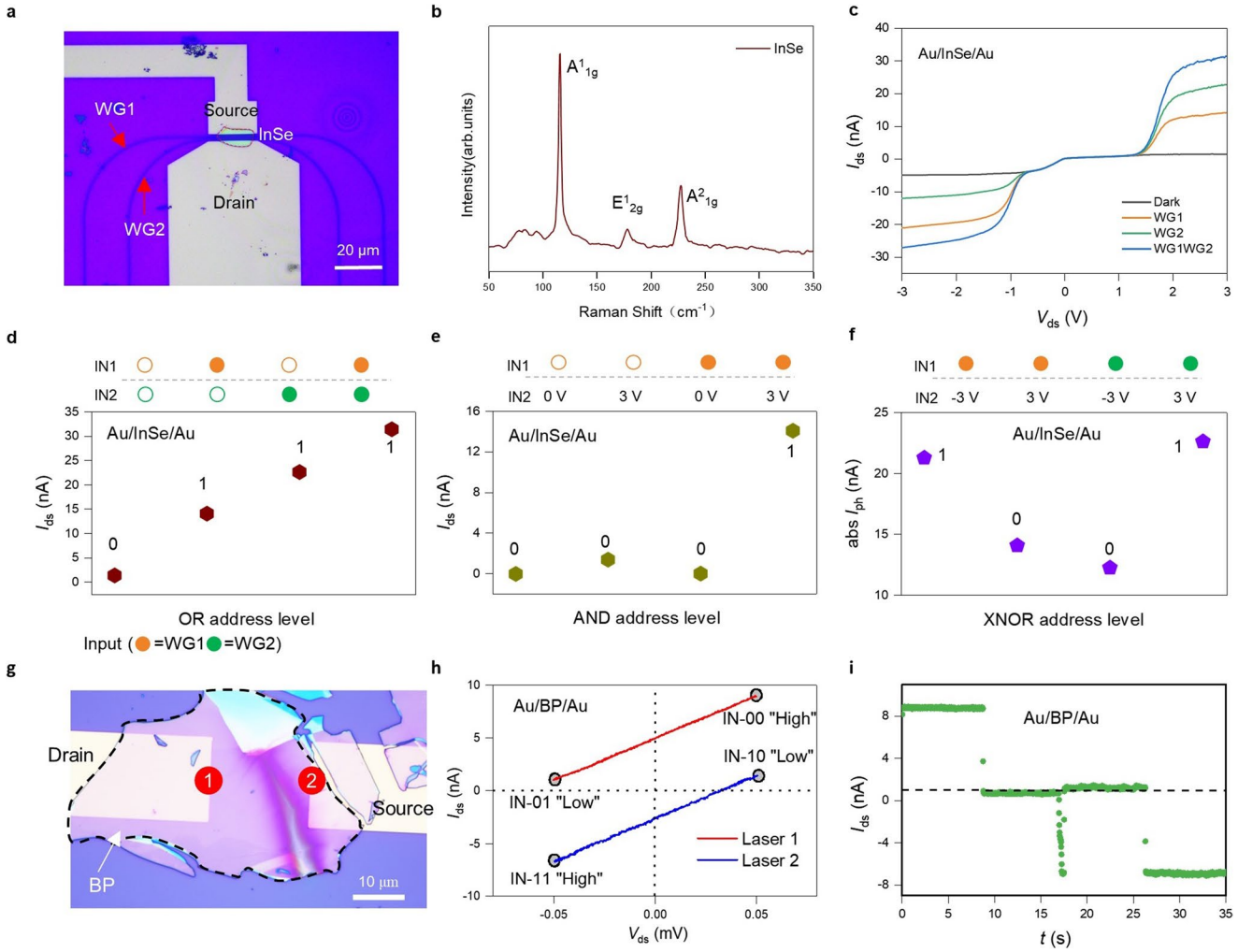
IN1	IN2	XNOR	IN1	IN2	Output
0	0	1	CH3	$-V_{oc}$	
0	1	0	CH3	$+V_{oc}$	
1	0	0	CH1	$-V_{oc}$	
1	1	1	CH1	$+V_{oc}$	

IN1	IN2	NAND	IN1	IN2	Output
0	0	1	CH2	$-V_{oc}$	
0	1	1	CH2	$+V_{oc}$	
1	0	1	CH3	$-V_{oc}$	
1	1	0	CH3	$+V_{oc}$	

IN1	IN2	NOR	IN1	IN2	Output
0	0	1	CH3	$-V_{oc}$	
0	1	0	CH3	$+V_{oc}$	
1	0	0	Dark	$-V_{oc}$	
1	1	0	Dark	$+V_{oc}$	

Extended Data Fig. 7 | Logic XNOR, NAND, NOR, and NOT gates. (a) Fiber-coupled measurement system. A tunable light (Santec TSL 550) was used as the source and amplified by EDFA. The light was coupled to the grating coupler in a chip, and the rest light was monitored by a power meter. Device was biased by a source meter (Keithley 2450). Two light beams with the same power was obtained with a 1×2 optical fiber splitter. The optical switch was used to open or close the optical circuits. (b) Output characteristic curves of Au/BP/Au device with three waveguides. Design scheme of (c) logic XNOR gate, (d) logic NAND gate, (e) logic NOR gate, and (f) logic NOT gate. For NOT gate, WG3 serve as input 1. The input signal with the value of 0 or 1 indicates zero and high light power. The high and low output current represent OUT-1 and OUT-0, respectively. When sequence signals (IN-0, IN-1, bias of Voc) are sent, a logic NOT gate can be constructed.

https://doi.org/10.1038/s41566-023-01309-7



Extended Data Fig. 8 | Integrated Au/InSe/Au and Au/BP/Au under free space for OELGs. (a) Optical microscopy image of Au/InSe/Au device. (b) Raman spectrum of the InSe. (c) Output characteristic curves of Au/InSe/Au device in the dark and under 1.55 μm light illumination. It is found that OR, AND, and XNOR logic functions can be constructed in the integrated Au/BP/Au device. (d) Output current for four states of logic OR gate with all-optical inputs at a bias voltage of 3 V. (e) Output current for four input states with mixed optical and electrical inputs. (f) Output current for four input states of logic XNOR gate with mixed optical and electrical inputs. (g) Optical microscopy image of Au/BP/Au device without integrating with waveguides. The red circles mean the position of the localized light spot. (h) Output characteristics of Au/BP/Au device under spot illumination. (i) Output current for four input states of logic XNOR gate with mixed optical and electrical inputs.

https://doi.org/10.1038/s41566-023-01309-7

Extended Data Table 1 | Performance comparison between MoS2/BP/MoS2 OELG and reported optoelectronic logic devices

Photodetector	Wavelength (nm)	Bias voltage (V)	Responsivity	Bandwidth (Hz)	Gain bandwidth product	Ref.
Carbon nanotube-Si	650	-3	1 A/W	/	/	20
CSi-PSi	658	5	21 mA/W	1.25×10^4	1.25×10^4	14
$CsCu_2I_3$	300/350	5	81.3 A/W	0.027	2.08×10^3	15
Bi_2O_2Se-Gra	365/635	1	110 A/W	/	/	42
CdSe-ZnS QDs	635	5	10.7 mA/W	/	/	17
GaN Nanowire	325	1	10^4 A/W	13.5	8.1×10^5	13
Graphene	800	/	/	/	/	19
MoS_2	514					18
Perovskite QDs	430					16
MoS_2/PZT	532					5
Perovskite	625/940	0	8.7 mA/W	514	514	41
$CuInS_2$-TiO_2	365/475		44.8 mA/W	175	175	43
MoS_2/BP/MoS_2	1550		0.35 A/W	2.3×10^8	2.3×10^8	This work

https://doi.org/10.1038/s41566-023-01309-7

Extended Data Table 2 | Function comparison between on-chip integrated OELGs and reported discrete optoelectronic logic devices

Materials	Wavelength (nm)	No. of Device							On-Chip	Ref.
		AND	OR	NOT	XOR	NAND	NOR	XNOR		
Carbon nanotube-Si	650	1	1	/	/	/	/	/	X	[20]
CSi-PSi	658	1	1	/	/	1	/	/	X	[14]
Graphene	800	1	1	/	/	1	1	/	X	[19]
MoS_2	514	/	/	/	/	1	/	/	X	[18]
Perovskite	625/940	2	2	2	/	2	2	/	X	[41]
Perovskite QDs	430	1	/	/	/	/	/	/	X	[16]
$CsCu_2I_3$	300/350	2	2	/	/	/	/	/	X	[15]
MoS_2/PZT	532	2	/	/	/	/	/	/	X	[5]
Bi_2O_2Se-Gra	365/635	2	2	/	/	/	/	/	X	[42]
$CuInS_2$-TiO_2	365/475	/	2	/	/	/	/	/	X	[43]
CdSe-ZnS QDs	635	/	/	1	/	2	2	/	X	[17]
GaN Nanowire	325	2	2	/	/	/	/	/	X	[13]
CMOS logic gates	-	2	2	2	12	4	4	14	-	
BP	1550	1	1	1	1	1	1	1	√	This work